SPECIFICATION

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[SOLDER PADS FOR IMPROVING RELIABILITY OF A PACKAGE]

Background of Invention

[0001] 1. Field of the Invention

[0002] The present invention relates to solder pads of a package, and more particularly, to solder pads for improving reliability of a package.

[0003] 2. Description of the Prior Art

[0004] High performance microelectronic devices often use solder balls or solder bumps for electrically and mechanically interconnection to other microelectronic devices. For instance, a very large scale integration (VLSI) chip may be connected to a circuit board or other next level packaging substrate by using solder balls or solder bumps. This connection technology is also referred to as "flip chip" technology. The flip chip technology is an area array connection technology and includes reflowing a body of solder onto a bond pad to form a solder bump, so as to electrically connect an IC die to a packaging board. The flip chip can break through limitations of traditional wire bonding, and the electrical performance is effectively improved due to a shorter connection pass.

[0005] Please refer to Fig.1. Fig.1 is a schematic diagram of a prior art package. As shown in Fig.1, a package 10 comprises a chip 12 and a substrate 18. The chip comprises a plurality of solder bump pads respectively connecting to the corresponding solder bumps 16. The solder bump pads 14 connect to the substrate 18 by using the solder bumps 16. In addition, an underfill layer 20 is filled in a gap between the chip 12 and the substrate 18 for tightly connecting the chip 12 with the substrate 18.

[0006] According to the prior art package technology, the substrate 18 comprises a

plastic (organic) substrate or a ceramic substrate. However, a price of the ceramic substrate is high and a source of the ceramic substrate is limited, so that the plastic substrate with a low price and plentiful sources has become a mainstream material used in packages. Nevertheless, a problem of non-uniform thermal stress always occurs in a package when using the plastic substrate. For example, a coefficient of thermal expansion of the chip 12 is approximately equal to 2.7 ppm/^{0}C, and a coefficient of thermal expansion of the plastic substrate 18 is approximately equal to 17 ppm/^{0}C. Because the chip 12 and the plastic substrate 18 have different coefficients of thermal expansion, a variation of ambient temperature deforms the package, and moreover, the products may fail.

[0007] Please refer to Fig.2(A) and Fig.2(B). Fig.2(A) and Fig.2(B) are a schematic diagrams for illustrating deformation of a package due to a variation of ambient temperature. As mentioned above, the coefficient of thermal expansion of the plastic substrate 18 is larger than that of the chip 12. When ambient temperature rises, the package 10 is bended upwards due to over expansion of the plastic substrate 18, as shown in Fig.2 (A). Conversely, when ambient temperature falls, the package 10 is bended downwards because the plastic substrate 18 shrinks more than the chip 12 does, as shown in Fig.2(B). Noticeably, a periphery region of the chip 12 is a region with high thermal stress. As a result, the deformation of the periphery region is more serious than the deformation of the central region of the chip 12, which further leads to forming cracks in the package.

[0008] For preventing deformation of the package due to a thermal stress, arrangement of the solder bump pads 14 for connecting the chip 12 with the substrate 18 is changed according to the prior art method. That is, positions of the solder bumps 16 are changed to adjust stress distribution on the chip 12 and the substrate 18. Please refer to Fig.3 and Fig.4. Fig.3 and Fig.4 are schematic diagrams of the solder bump pads located on the surface of the chip. Generally, the solder bump pads are arranged in a matrix on the chip. For explaining the relationship between positions of the solder bump pads and the stress on the chip, Fig.3 and Fig.4 only show solder bump pads located on the region of the chip with high stress (i.e. periphery region). As shown in Fig.3, the solder bump pads 14 are arranged in a matrix on the chip 12. When ambient temperature varies, the largest thermal stress always occurs on a

position of the chip 12 with a maximum distance to neutral point (max DNP). For example, the solder bump pads 22 located at the four corners of the chip 12 are suffered with higher thermal stress, so that the package forms cracks most easily on the positions of the solder bump pads 22. As shown in Fig.4, the solder bump pads 22 are directly removed to solve the above-mentioned problem according to the prior art method. That is, it is avoided to locate the solder bump pads and the solder bumps at the corners of the chip 12, which is called a bump corner design rule.

[0009] As mentioned above, the prior art method removes the solder bump pads 14 located at the four corners of the chip 12. However, the solder bump pads 14 on other high stress regions of the chip 12 are not removed. For example, the solder bump pads 24 shown in Fig.4 also suffer from higher stress. As a result, as the chip 12 becomes larger, the above-mentioned method cannot effectively solve the thermal stress problem, and thus, reliability of the package is reduced.

Summary of Invention

[0010] It is therefore a primary objective of the claimed invention to provide solder pads for improving reliability of a package.

[0011] According to the claimed invention, solder pads for improving reliability of a semiconductor package are provided. The package includes a substrate and/or a chip. The solder pad includes a plurality of first solder pads located on a surface of the substrate and/or the chip, and at least a second solder pad located on a predetermined region of the surface of the substrate and/or the chip. Each of the first solder pads has a first diameter. The second solder pad has a second diameter greater than the first diameter so as to sustain a stronger thermal stress on the substrate and/or the chip.

[0012]

It is an advantage over the prior art that the solder pads with larger sizes are located on the high stress regions of substrate and/or the chip in the claimed invention. The solder pads with larger sizes can sustain stronger thermal stress and mechanical strength. Thus, the claimed invention provides solder pads capable of effectively improving reliability of a package. In addition, the claimed invention controls the sizes of the solder pads by adjusting the sizes of the openings of the

photoresist layer in the solder pad process. Thus, it is achievable to improve reliability of the package without adding additional processes and equipment or changing original processes.

[0013] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment, which is illustrated in the multiple figures and drawings.

Brief Description of Drawings

[0014] Fig.1 is a schematic diagram of a prior art package.

[0015] Fig.2(A) and Fig.2(B) are a schematic diagrams for illustrating deformation of a package due to a variation of ambient temperature.

[0016] Fig.3 and Fig.4 are schematic diagrams of the solder bump pads located on the surface of the chip according to the prior art.

[0017] Fig.5 to Fig.11 are schematic diagrams for illustrating the solder pads of the embodiments according to the present invention.

[0018] Fig.12 is a schematic diagram of a package according to the present invention.

Detailed Description

[0019]

Please refer to Fig.5 to Fig.11. Fig.5 to Fig.11 are schematic diagrams for illustrating the solder pads of the embodiments according to the present invention. The solder pads with larger sizes are located on the high stress regions of a substrate and/or a chip in the present invention. The solder pads with larger sizes can sustain stronger thermal stress and mechanical strength. As shown in Fig.5, Fig.5 illustrates the solder pads of the first embodiment. A plurality of first solder pads 32 and a plurality of second solder pads 34 are located on a surface of a substrate and/or a chip 30. The first solder pads 32 are arranged in a matrix at a center region of the substrate 30. The second solder pads 34 are arranged at the four vertexes of the matrix formed by the first solder pads 32. The diameter of the second solder pad 34 is larger than that of the first solder pad 32. In order to ensure reliability of the package during the welding process, the height of the first solder pad 32 is equal or

approximately equal to that of the second solder pad 34.

[0020] Please refer to Fig.6. Fig.6 illustrates the solder pads of the second embodiment of the present invention. As shown in Fig.6, a plurality of first solder pads 32 and a plurality of second solder pads 34 are located on a surface of a substrate and/or a chip 30. The first solder pads 32 are arranged in a matrix at a center region of the substrate 30. The second solder pads 34 are located at the corners of the matrix formed by the first solder pads 32. In addition, the corners of the matrix include the four vertexes of the matrix and the positions around the vertexes of the matrix. The diameter of the second solder pad 34 is larger than that of the first solder pad 32. In order to ensure reliability of the package during the welding process, the height of the first solder pad 32 is equal or approximately equal to that of the second solder pad 34.

[0021] Please refer to Fig.7. Fig.7 illustrates the solder pads of the third embodiment of the present invention. As shown in Fig.7, a plurality of first solder pads 32 and a plurality of second solder pads 34 are located on a surface of a substrate and/or a chip 30. The first solder pads 32 are arranged in a matrix at a center region of the substrate and/or the chip 30. The second solder pads 34 are arranged at the regions near the four vertexes of the matrix formed by the first solder pads 32. For example, the second solder pads 34 are arranged at the positions around the four vertexes of the matrix, and no second solder pads 34 are located at the four vertexes of the matrix. The diameter of the second solder pad 34 is larger than that of the first solder pad 32. In order to ensure reliability of the package during the welding process, the height of the first solder pad 32 is equal or approximately equal to that of the second solder pad 34.

[0022] Please refer to Fig.8. Fig.8 illustrates the solder pads of the fourth embodiment of the present invention. As shown in Fig.8, a plurality of first solder pads 32 and a plurality of second solder pads 34 are located on a surface of a substrate and/or a chip 30. The first solder pads 32 are located at the four sides of the substrate and/or the chip 30 and the first solder pads 32 are arranged in a rectangle. The second solder pads 34 are located at the four vertexes of the rectangle formed by the first solder pads 32. The diameter of the second solder pad 34 is larger than that of the

first solder pad 32. In order to ensure reliability of the package during the welding process, the height of the first solder pad 32 is equal or approximately equal to that of the second solder pad 34.

[0023] Please refer to Fig.9. Fig.9 illustrates the solder pads of the fifth embodiment of the present invention. As shown in Fig.9, a plurality of first solder pads 32 and a plurality of second solder pads 34 are located on a surface of a substrate and/or a chip 30. The first solder pads 32 are located at the four sides of the substrate and/or the chip 30 and the first solder pads 32 are arranged in a rectangle. The second solder pads 34 are located at the regions near the four vertexes of the rectangle formed by the first solder pads 32. For example, the second solder pads 34 are arranged at the positions around the four vertexes of the rectangle, and no second solder pads 34 are located at the four vertexes of the rectangle. The diameter of the second solder pad 34 is larger than that of the first solder pad 32. In order to ensure reliability of the package during the welding process, the height of the first solder pad 32 is equal or approximately equal to that of the second solder pad 34.

[0024] Under ideal conditions, taking the center of the substrate and/or the chip as a center of a circle, the solder pads located at the circumference of the same concentric circle are suffered with approximately equal thermal stress. The present invention arranges solder pads with different sizes according to the above-mentioned stress distribution. Please refer to Fig.10. Fig.10 illustrates the solder pads of the sixth embodiment of the present invention. As shown in Fig.10, a plurality of first solder pads 32 and a plurality of second solder pads 34 are located on a surface of a substrate and/or a chip 30. The first solder pads 32 are located at circumferences of a plurality of concentric circles. The second solder pads 34 are located at a high stress region, which is farthest from the center of the substrate and/or the chip 30. That is, the second solder pads 34 are located at the circumference of the maximum circle on the substrate 30. The diameter of the second solder pad 34 is larger than that of the first solder pad 32. In order to ensure reliability of the package during the welding process, the height of the first solder pad 32 is equal or approximately equal to that of the second solder pad 34.

[0025]

Please refer to Fig.11. Fig.11 illustrates the solder pads of the seventh

embodiment of the present invention. As shown in Fig.11, a plurality of first solder pads 32 and a plurality of second solder pads 34 are located on a surface of a substrate 30. The first solder pads 32 are located at circumferences of a plurality of concentric circles. The second solder pads 34 are located at the corners outside theconcentric circles formed by the first solder pads 32. The diameter of the second solder pad 34 is larger than that of the first solder pad 32. In order to ensure reliability of the package during the welding process, the height of the first solder pad 32 is equal or approximately equal to that of the second solder pad 34.

[0026] The present invention can be applied not only in a flip-chip package, but also in a ball grid array (BGA) package. As a result, in all embodiments of the present invention, the substrate 30 can be a semiconductor wafer, and the first solder pads 32 and the second solder pads 34 can be solder bump pads for connecting the semiconductor wafer with the plastic substrate or the ceramic substrate. The substrate 30 comprises a plastic substrate, a ceramic substrate, or a printed circuit board. The first solder pads 32 and the second solder pads 34 are solder ball pads for connecting the above-mentioned substrate with other chips or substrates.

[0027] Please refer to Fig.12. Fig.12 is a schematic diagram of a package according to the present invention. As shown in Fig.12, a package 40 comprises a chip 42, a substrate 44, and a print circuit board 46. An underfill layer 56 is filled in a gap between the chip 42 and the substrate 44. The substrate 44 is a plastic substrate or a ceramic substrate. A plurality of solder bump pads 52 is located on a first surface of the substrate 44, and each solder bump pad 52 connects to a solder bump 54. The solder bump pads 52 connect to the chip 42 by use of the solder bumps 54. A plurality of solder ball pads 58 is located on a second surface of the substrate 44, and each solder ball pad 58 connects to a solder ball 60. The solder ball pads 58 connect to the print circuit board 46 by use of the solder balls 60. Noticeably, in order to make the package sustain higher thermal stress and higher fatigue strength, the solder bump pads 52 or the solder ball pads 58 should have at least two different kinds of diameters. The solder bump pads 52 or the solder ball pads 58 with larger sizes are used to sustain a stronger thermal stress during a thermal process. The arrangement of the solder bump pads 52 or the solder ball pads 58 can refer to the first embodiment to the seventh embodiment of the present invention.

[0028] In addition, the solder bump pads 52 can be located on a surface of the chip 42 in the package 40 shown in Fig.12. Then, each solder bump pad 52 connects to a solder bump 54, and uses the solder bump 54 to connect to the substrate 44. Conversely, the solder ball pads 58 can be located on a surface of the print circuit board 46. Each solder ball pad 58 connects to a solder ball 60, and uses the solder ball 60 to connect to the substrate 44.

[0029] In comparison with the prior art, the solder pads with larger sizes are located on the high stress regions of the substrate in the claimed invention. The solder pads with larger sizes can sustain stronger thermal stress and mechanical strength. Thus, the claimed invention provides solder pads capable of effectively improving reliability of a package. In addition, the claimed invention controls the sizes of the solder pads by adjusting the sizes of the openings of the photoresist layer in the solder pad process. Thus, it is achievable to improve reliability of the package without adding additional processes or changing original processes.

[0030] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bound of the appended claims.